DATA SHEET

GTL2002
Dual open drain voltage translator

Product specification

2000 Aug 16

Philips
Semiconductors

PHILIPS

Dual open drain voltage translator GTL2002

FEATURES

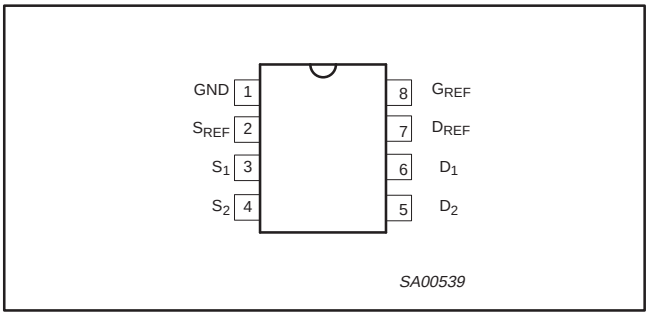
- Direct interface with TTL level
- 6.5 Ω ON-state connection between port S_n and D_n

DESCRIPTION

The GTL2002 is a high speed dual voltage translator. The low ON-state resistance of the clamp allows connections to be made with minimal propagation delay.

The device is organized as one 2-bit voltage clamp. When S or D is low, the clamp is in the ON-state and a low resistance connection exists between the S and D ports. When S port and D port are high, the clamp is in the OFF-state and a very high impedance exists between the S and D ports. When port D is high, the voltage on the S port is clamped to the applied reference voltage on the GREF port.

PIN CONFIGURATION



FUNCTION TABLE

G_{REF}	D_{REF}	S_{REF}[4]	Switch	Driven Input[5]	Output of Driven Input
H	H	0 V	off	> 0 V	H[2]
H	H	V_{TT}	nearly off	H	V_{TT}[1]
H	H	V_{TT}	nearly off	V_{TT}	H[2]
H	H	V_{TT}	on	L	L[2,3]
L	L	0 – V_{TT}	off	X	H[2]

H = High voltage level
L = Low voltage level
X = Don't Care
V_{TT} = Termination voltage, typically 1.5 V

NOTES:
1. The output is not pulled up or pulled down.
2. The output is pulled up to V_{CC} through an external resistor.
3. The output of driven input follows the input low.
4. G_{REF} must be at least 1.5 V higher than S_{REF} for proper switch operation.
5. Either S_n or D_n can be chosen as the input; the corresponding D_n or S_n will be the output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH}	Propagation delay Sn to Dn	V_{DD1} = 3.3 V; V_{DD2} = 2.5 V; V_{REF} = 1.5 V; unloaded	1.5	ns
C_{OFF}	Channel capacitance (OFF-state)	V_S = 1.5 V	7.5	pF

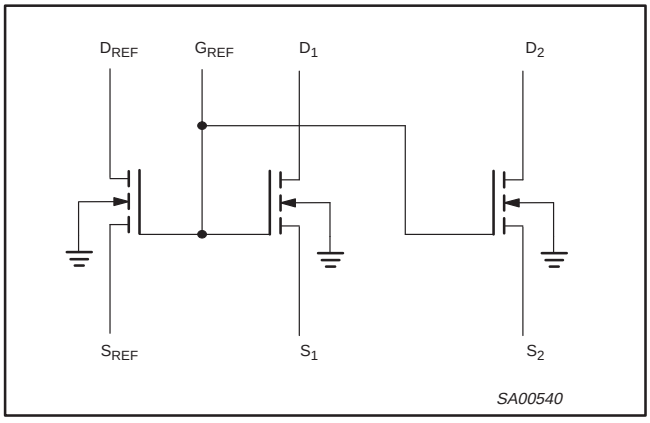
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
8-Pin Plastic SO	0°C to +85°C	GTL2002D	SOT96-1
8-Pin Plastic TSSOP	0°C to +85°C	GTL2002DP	SOT505-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	GND	Ground (0V)
2	S_{REF}	Source of reference transistor
3, 4	S_n	Port S_1 to Port S_2
5, 6	D_n	Port D_1 to Port D_2
7	D_{REF}	Drain of reference transistor
8	G_{REF}	Gate of reference transistor

CLAMP SCHEMATIC



ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{S_REF}	DC source reference voltage		–0.5 to +7.0	V
V_{D_REF}	DC drain reference voltage		–0.5 to +7.0	V
V_{G_REF}	DC gate reference voltage		–0.5 to +7.0	V
V_{Sn}	DC voltage Port S_n		–0.5 to +7.0	V
V_{Dn}	DC voltage Port D_n		–0.5 to +7.0	V
I_{REFK}	DC reference diode current	$V_I < 0$	–50	mA
I_{SK}	DC diode current Port S_n	$V_I < 0$	–50	mA
I_{DK}	DC diode current Port D_n	$V_I < 0$	–50	mA
I_{MAX}	DC clamp current per channel	Channel in ON-state	±35	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{S_REF}	DC source reference voltage		1.0	4.4	V
V_{D_REF}	DC drain reference voltage		V_{S_REF} + 0.6	5	V
V_{G_REF}	DC gate reference voltage		V_{S_REF} + 0.6	5	V
V_{Sn}	DC voltage Port S_n (OFF-state)		V_{S_REF}	5	V
V_{Sn}	DC voltage Port S_n (ON-state)		0	0.2	V
V_{Dn}	DC voltage Port D_n (OFF-state)		V_{S_REF}	5	V
V_{Dn}	DC voltage Port D_n (ON-state)		0	0.4	V
I_S	Switch input leakage current (OFF-state) for S_n and D_n I/O	V_S, V_D = 5 V		15	µA
I_I	G_{REF} input leakage current	V_G = 5 V		2.5	µA
T_{amb}	Operating ambient temperature range	In free air	0	+85	°C

DC CHARACTERISTICS for V_{DD1} = 3.0 to 3.6 V; V_{DD2} = 2.36 to 2.64 V; V_{REF} = 1.365 to 1.635 V range

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V). Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = 0°C to +85°C			
			Min	Typ[1]	Max	
V_{OL}	LOW level output voltage	V_S = 0.175 V; I_{CLAMP} = 15.2 mA		260	350	mV

NOTE:

1. All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{REF} = 1.5 V and T_{amb} = 25°C.

AC CHARACTERISTICS for V_{DD1} = 3.0 to 3.6 V; V_{DD2} = 2.36 to 2.64 V; V_{REF} = 1.365 to 1.635 V range

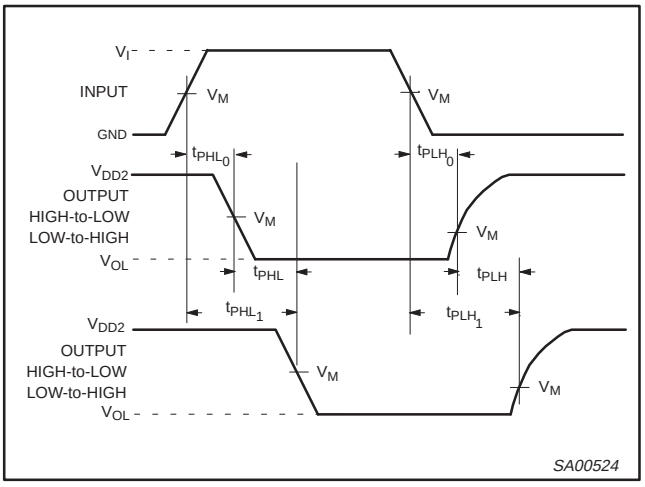
GND = 0 V; $t_r = t_f \leq 3.0$ ns. Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = 0 to +85°C			
			MIN	TYP[1]	MAX	
t_{PLH}[2]	Propagation delay Sn to Dn; Dn to Sn		0.5	1.5	5.5	ns

NOTES:

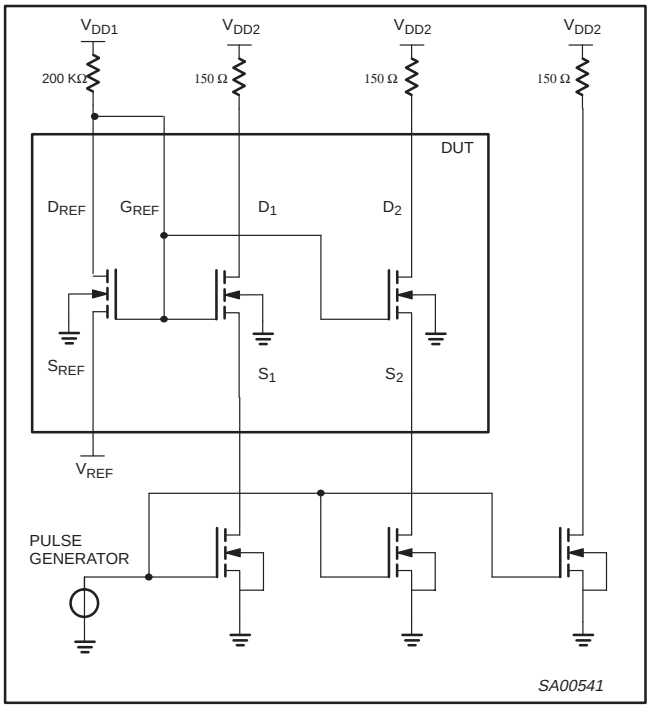
1. All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{REF} = 1.5 V and T_{amb} = 25°C.
2. Propagation delay guaranteed by characterization.
3. $C_{ON,MAX}$ of 30 pF and a $C_{OFF,MAX}$ of 15 pF is guaranteed by design.

AC WAVEFORMS



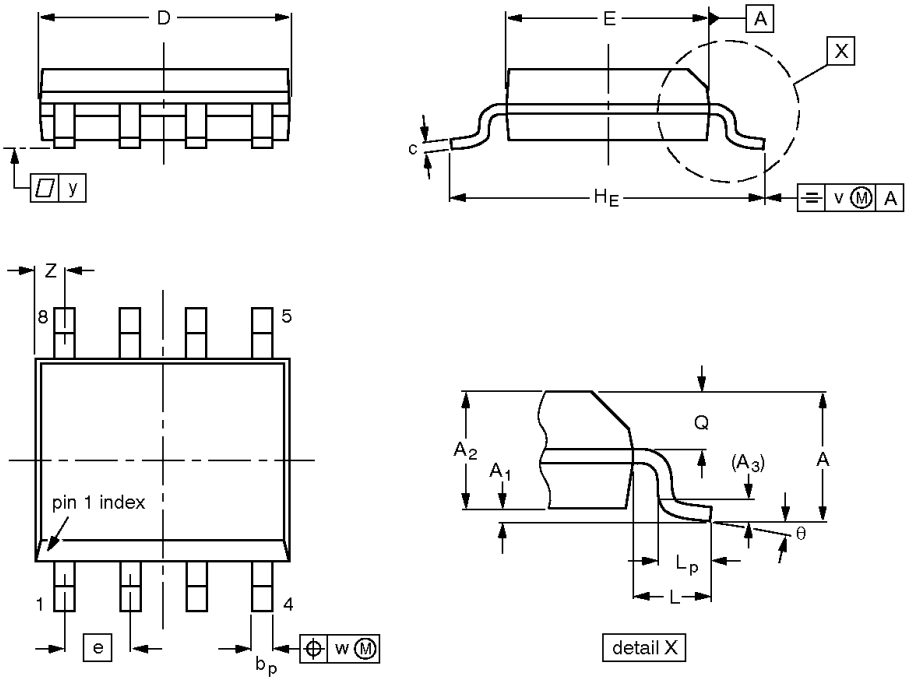
Waveform 1. The Input (S_n) to Output (D_n) Propagation Delays

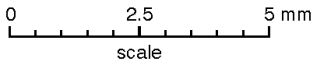
TEST CIRCUIT



Waveform 2. Load circuit

SO8: plastic small outline package; 8 leads; body width 3.9mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

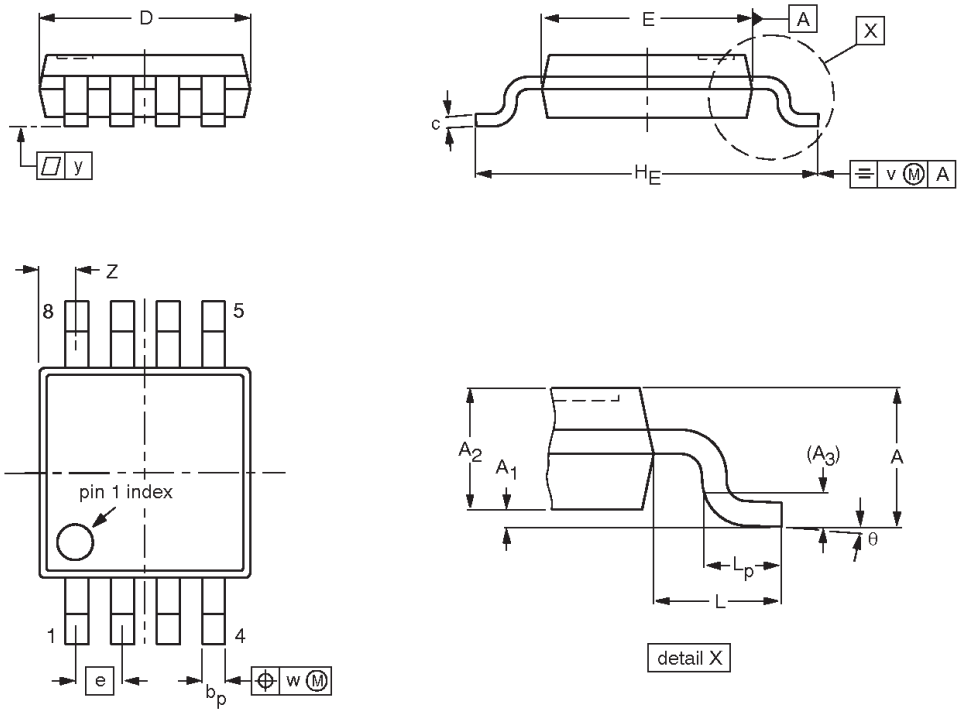
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

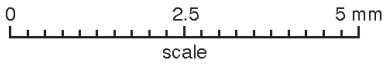
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

Date of release: 08-00

Document order number: 9397 750 07417

Let's make things better.

Philips Semiconductors

PHILIPS